REMARKS

Claims 38 and 39 are all the claims presently pending in the application. Claims 38 and 39 are amended to more particularly define the invention. No new matter is added.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 38 stands provisionally rejected on the ground of nonstatutory double patenting over claims 1-7 and 34-36 of copending Application No. 12/062,211. However, while Applicants respectfully disagree, to expedite prosecution, claims 38 is amended to alleviate the Examiner's concerns and render the double patenting rejection to be moot.

Claims 38 and 39 stand rejected under 35 U.S.C. § 112, second paragraph as being allegedly indefinite. However, while Applicants disagree with the rejections, to expedite prosecution, claims 38 and 39 are amended to alleviate the Examiner's concerns and render the informality rejections to be moot.

In addition, with respect to claim 39, Applicants respectfully assume that the Examiner declined to examine claim 39 in view of the prior art, as the only rejection issued by the Examiner with respect to claim 39 is the above-referenced informality rejection. Indeed, the Examiner failed to indicate any double patenting or prior art rejection with respect to claim 39. Applicants respectfully request clarification if this assumption is incorrect. Applicants also respectfully submit that claim 39 was and is in condition for examination on its merits with respect to the prior art.

With respect to the prior art, claim 38 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Dai (U.S. Patent Publication No. 2005/0049848 A1) in view of Autrey et al. (U.S. Patent No. 5,774,695).

This rejection is are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

An exemplary aspect of the claimed invention (e.g., as recited in claim 38) is directed to a computer system, including a local area network (LAN), a plurality of computers without on-board

user interface controllers, each of the plurality of computers being coupled to the LAN and being in communication with each other over the LAN, each of the plurality of computers including at least one central processing unit (CPU) and a system controller being coupled to the at least one CPU, a console including a user input device and a user output device, the console being coupled to communicate over the LAN such that the console encapsulates an input received via the user input device into incoming data frames, conveys the incoming data frames over the LAN to each of the plurality of computers, de-encapsulates outgoing data frames received by the console from each of the plurality of computers over the LAN into an output for display using the user output device, and a plurality of input/output (I/O) devices being coupled to the LAN, the plurality of I/O devices including the user input device and the user output device of the console, each of the plurality of computers being in communication with the plurality of I/O devices over the LAN. The plurality of computers and the console are arranged to communicate over the LAN by transmitting Layer 2 data frames. The plurality of computers and the console are arranged to convey the input and the output by tunneling over Layer 2 on the LAN. The plurality of computers and the console are arranged to encapsulate the input and output in Internet Protocol (IP) packets for transmission over the LAN. The plurality of computers and the console are arranged to encapsulate the input and output using an application-layer protocol. The plurality of computers are arranged to transmit the outgoing data frames over the LAN to the plurality of I/O devices. Each of the plurality of computers further includes a plurality of on-board I/O device controllers, consisting of at least one LAN interface being directly coupled to the LAN and connected to the system controller, and an emulation processor, the emulation processor being directly coupled to the system controller, the emulation device including I/O trap logic being directly coupled to the system controller, the I/O trap logic being configured to intercept and trap a plurality of outputs sent by the at least one CPU to the plurality of I/O devices, to pass a plurality of inputs received from a service processor of the emulation device to the at least one CPU via the system controller, and to emulate behavior of the plurality of I/O devices to the at least one CPU and the system controller, and the service processor being directly coupled to the I/O trap logic, the service processor being configured to receive the intercepted and trapped plurality of outputs from the I/O trap logic, to encapsulate the received plurality of outputs into the outgoing data frames, to transmit the outgoing data frames via the at least one LAN interface through the LAN for delivery to the plurality of I/O devices, to receive the incoming data frames via the at least one LAN

interface sent by the plurality of I/O devices through the LAN, to de-encapsulate the received incoming data frames into the plurality of inputs, and to convey the plurality of inputs to the I/O trap logic for emulation to the at least one CPU via the system controller. The emulation processor is arranged to encapsulate the plurality of outputs in Ethernet frames. The emulation processor is arranged to encapsulate the plurality of outputs in Internet Protocol (IP) packets. The emulation processor is arranged to encapsulate the plurality of outputs using an application-layer protocol.

A number of new standards have recently been promulgated to permit accessing at least some I/O peripherals remotely, via packet networks. However, conventional computer systems are not oriented in such a way as to accommodate such a structure. (Application at page 1, line 13 to page 2, line 10).

An exemplary embodiment of the claimed invention, on the other hand, is directed to a computer system, where each of the plurality of computers further includes a plurality of on-board I/O device controllers, consisting of at least one LAN interface being directly coupled to the LAN and connected to the system controller, and an emulation processor, the emulation processor being directly coupled to the system controller, the emulation device including I/O trap logic being directly coupled to the system controller, the I/O trap logic being configured to intercept and trap a plurality of outputs sent by the at least one CPU to the plurality of I/O devices, to pass a plurality of inputs received from a service processor of the emulation device to the at least one CPU via the system controller, and to emulate behavior of the plurality of I/O devices to the at least one CPU and the system controller, and the service processor being directly coupled to the I/O trap logic, the service processor being configured to receive the intercepted and trapped plurality of outputs from the I/O trap logic, to encapsulate the received plurality of outputs into the outgoing data frames, to transmit the outgoing data frames via the at least one LAN interface through the LAN for delivery to the plurality of I/O devices, to receive the incoming data frames via the at least one LAN interface sent by the plurality of I/O devices through the LAN, to de-encapsulate the received incoming data frames into the plurality of inputs, and to convey the plurality of inputs to the I/O trap logic for emulation to the at least one CPU via the system controller. (Application at page 10, line 17 to page 12, line 2). This exemplary feature may provide a computer system having substantially increased board space and reduced power requirements, complexity, cost, and management effort. (Application at page 2, lines 25-29).

II. THE PRIOR ART REJECTION – The Alleged Dai and Autrey Combination

Dai discloses mechanisms that allow a physical storage device that has storage capability to emulate one or more storage devices. (Dai at Abstract). Autrey discloses a protocol interface gateway connecting a telecommunication system emulator to a communications network. (Autrey at Abstract). The Examiner alleges that the combination of Dai and Autrey makes the claimed invention obvious.

However, even assuming (arguendo) one of ordinary skill in the art would combine Dai and Autrey, the resultant combination fails to teach or suggest each and every feature of the claimed invention. Specifically, Dai and Autrey – either alone or assuming (arguendo) combination – clearly fail to teach or suggest a computer system, "*wherein each of the plurality of computers further comprises a plurality of on-board I/O device controllers, consisting of . . . at least one LAN interface being directly coupled to the LAN and connected to the system controller; and an emulation processor, said emulation processor being directly coupled to the system controller, the emulation device comprising . . . I/O trap logic being directly coupled to the system controller, the I/O trap logic being configured to intercept and trap a plurality of outputs sent by the at least one CPU to the plurality of I/O devices, to pass a plurality of inputs received from a service processor of the emulation device to the at least one CPU via the system controller, and to emulate behavior of the plurality of I/O devices to the at least one CPU and the system controller; and the service processor being directly coupled to the I/O trap logic, the service processor being configured to receive the intercepted and trapped plurality of outputs from the I/O trap logic, to encapsulate the received plurality of outputs into the outgoing data frames, to transmit the outgoing data frames via the at least one LAN interface through the LAN for delivery to the plurality of I/O devices, to receive the incoming data frames via the at least one LAN interface sent by the plurality of I/O devices through the LAN, to de-encapsulate the received incoming data frames into the plurality of inputs, and to convey the plurality of inputs to the I/O trap logic for emulation to the at least one CPU via the system controller*", as recited, for example, in claim 38 (Application at page 8, line 13 to page 9, line 3). As previously mentioned, this exemplary feature may provide a computer system having substantially increased board space and reduced power requirements, complexity, cost, and management effort (Application at page 2, lines 25-29).

The Examiner alleges that paragraphs [0033]-[0035] and [0054] of Dai teach the emulation device of the claimed invention. (Office Action at page 9, point 17). Applicants respectfully disagree. Dai only teaches an emulation device of an I/O device, which, in this case, is physical storage device 220. Further, Dai clearly fails to teach or suggest the structure of the computer system of the claimed invention, including that of the role that the emulation device plays within the computer system of the claimed invention. Indeed, Dai clearly fails to teach or suggest the above-referenced exemplary feature of the claimed invention.

To make up for the deficiencies of Dai, the Examiner applies Autrey. The Examiner alleges that, at column 2, lines 13-25 and column 8, lines 3-24, "Autrey teaches the computers and the console are arranged to encapsulate the input and output using an application-layer protocol. (Office Action at page 10, point 26). However, like Dai, Autrey clearly fails to teach or suggest the structure of the computer system of the claimed invention, including that of the role that the emulation device plays within the computer system of the claimed invention. Indeed, the alleged combination of Dai and Autrey clearly fails to teach or suggest the above-referenced exemplary feature of the claimed invention. Thus, the Examiner fails to make a *prima facie* case of obviousness with respect to the claimed invention.

Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 38 and 39, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, Applicants request the Examiner to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The undersigned authorizes the Commissioner to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: March 10, 2010

McGinn IP Law Group, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182-3817
(703) 761-4100
Customer No. 48150

Christopher R. Monday
Registration No. 60,929

Sean M. McGinn
Registration No. 34,386